Mixed signal Design using cadence :

Due to some debug in the file system,not all the setups in cadence is able to perform this operationOnly one setup is giving the correct result.For that,you need to type the following commands

. cadence2009

. caliber-setup-new

Tcsh

Cd cadence

Source setup-cadence

Virtuoso &

This tutorial aims at using the virtuoso for performing a mixed signal design using a NAND gate (written in verilog) and an inverter (drawn in schematic ) and perform the simulation using spectre-verilog .

* Create a new library and in a new cell view,make an inverter in schematic.Generate the symbol and save it.
* In the same library,make a new cell view,named NAND\_hdl.choose verilog as the type and give a view name. Write the verilog code of NAND gate and save it.If the design does not have any error,then as soon as you close the file,a message will appear to make the symbol view of the NAND gate. This will create the symbol that can be inserted into the schematics along with inverter.
* In the same library,make a new cell view named design\_try and choose schematic as the type.In that schematic ,insert the Nand gate and the inverter made before.make the necessary coonections.If NAND gate is placed before the inverter,that means the input stimuli will be digital.Hence you need to create the Vdd connection for the analog part (here it is the inverter).insert vdd,vdc and gnd and fix the value of the vdd as per the technology.check and save the design
* Make another cell view,the same as the one above ie design\_try.But this time chose config as the type.This will open up a window.In that select the view as schematic. Down in the window,there will be the option of use template. Clicking on that will ask for an option of the type of simulator you want to use.select spectre verilog instead of spectre and clock ok. This will give you the hierarchial view of the different components being used in the design.In the toolbar,select view->update.Then save the config and close.
* Once you have closed it,you have to open it once again.The first thing that will appear where it will ask for the views you want to see. click yes on both the options.This will setup the switch view list order for simulation.
* Inside the config,switch over to tree view instead of table view.There,for the schematic portion (ie the inverter) ,right click on it, select view to use as schematic and inherited view list as spectre.you need to click on the inherited view list,then type spectre by hand.For the rest,ie the verilog part and the analog library module,leave it as default. Again view->update and save the config.
* Then go to the schematic part of that config and open the ADE-L from there.It is same as the ADE-L from schematic,just that instead of schematic view,it is the config view.
* Go to simulator,change it to spectre-verilog.Add model library,go to the stimuli,select digital (since the first gate is NAND).Modify the verilog testbench and save it.Go back to cofig schematic.select mixed signal option from the launch option.select verimix.That will be automaticallt selected on upper the tool bar.Go inside the verimix,select partitioning and select all active.This will show you the different kinds of simulation being performed,the NAND gate being verilog,the inverter being spectre and the other being schematic.
* Still in the verimix,select interface->library.This shows the a-d and d-a converter required for interfacing between the 2 domains.for a-d,select 5 and 0 for high and low.for d-a,select 1.2v and 0 for high and low (this depends on your technology)
* Now you are all set for the simulation.